

What is claimed is:

1 1. A method of forming a double-gate transistor comprising the steps of:
2 providing a semiconductor wafer having a substrate and a device layer, a
3 back gate dielectric layer adjacent to and below said Device layer, a back
4 gate electrode between said back gate dielectric layer and said substrate, a
5 front gate dielectric on said Device layer and a front gate electrode layer on
6 said front gate dielectric layer;
7 depositing at least one transfer layer on said front gate electrode layer;
8 patterning said at least one transfer layer with a gate pattern and forming a
9 first gate in said front gate electrode layer using said transfer layer as a mask;
10 forming at least one vertical spacer layer adjacent to opposite sides of said
11 front gate;
12 etching said Device layer using said at least one spacer layer as a mask to
13 form a transistor body disposed on said back gate dielectric layer;
14 oxidizing said back gate electrode such that oxide is formed below said
15 transistor body and on either side of a central portion of said back gate
16 electrode, thereby forming said back gate self-aligned with said front gate;
17 and
18 forming source and drain electrodes on opposite sides of said transistor body.

1 2. A method according to claim 1, in which said step of forming at least
2 one vertical spacer comprises forming a first vertical spacer in proximity to
3 said front gate and having a bottom surface above said transistor body;
4 thereafter performing said step of etching said Device layer to form said

5 transistor body; and
6 forming a second spacer in proximity to a vertical edge of said transistor
7 body.

1 3. A method according to claim 1, in which said step of oxidizing said
2 back gate electrode is performed with at least one vertical spacer disposed in
3 proximity to a vertical edge of said transistor body, thereby defining a lateral
4 extent of oxidation by the thickness of said vertical spacer, said oxidation
5 extending underneath said vertical spacer and said transistor body and into
6 said back gate electrode.

1 4. A method according to claim 2, in which said step of oxidizing said
2 back gate electrode is performed with said second vertical spacer disposed in
3 proximity to a vertical edge of said transistor body, thereby defining a lateral
4 extent of oxidation by the thickness of said second vertical spacer, said
5 oxidation extending underneath said vertical spacer and said transistor body
6 and into said back gate electrode.

1 5. A method according to claim 1, further comprising a step of
2 depositing a layer of interlevel dielectric about said transistor up to at least
3 the top of said front gate, stripping said second vertical spacer, thereby
4 forming an aperture over the source and drain of said transistor, and
5 depositing a conductive material in said aperture, thereby forming a raised
6 S/D structure.

- 1 6. A method according to claim 1, in which said step of oxidizing is
2 conducted at a temperature of at least 1000 degrees Centigrade for a time
3 sufficient to reduce stress in said transistor body.
- 1 7. A method according to claim 1, in which said step of oxidizing is
2 conducted at a temperature of at least 1000 degrees Centigrade for at least
3 twenty minutes.
- 1 8. A method according to claim 2, in which said step of oxidizing is
2 conducted at a temperature of at least 1000 degrees Centigrade for at least
3 twenty minutes.
- 1 9. A method according to claim 1, further comprising a step of
2 performing an angled implantation into said back gate electrode of an ion
3 species that promotes oxidation before said step of oxidation, thereby
4 increasing the rate of oxidation in the implanted area.
- 1 10. A method according to claim 2, further comprising a step of
2 performing an angled implantation into said back gate electrode of an ion
3 species that promotes oxidation before said step of oxidation, thereby
4 increasing the rate of oxidation in the implanted area.
- 1 11. A method according to claim 4, further comprising a step of
2 performing an angled implantation into said back gate electrode of an ion

3 species that promotes oxidation before said step of oxidation, thereby
4 increasing the rate of oxidation in the implanted area.

1 12. A method according to claim 6, further comprising a step of
2 performing an angled implantation into said back gate electrode of an ion
3 species that promotes oxidation before said step of oxidation, thereby
4 increasing the rate of oxidation in the implanted area.

1 13. A method according to claim 7, further comprising a step of
2 performing an angled implantation into said back gate electrode of an ion
3 species that promotes oxidation before said step of oxidation, thereby
4 increasing the rate of oxidation in the implanted area.

1 14. A method according to claim 1, further comprising a step of
2 performing a vertical implantation into said back gate electrode of an ion
3 species that retards oxidation before said step of oxidation, thereby
4 decreasing the rate of oxidation in the vertical direction.

1 15. A method according to claim 6, further comprising a step of
2 performing a vertical implantation into said back gate electrode of an ion
3 species that retards oxidation before said step of oxidation, thereby
4 decreasing the rate of oxidation in the vertical direction.

1 16. A method according to claim 7, further comprising a step of
2 performing a vertical implantation into said back gate electrode of an ion

3 species that retards oxidation before said step of oxidation, thereby
4 decreasing the rate of oxidation in the vertical direction.

1 17. A method according to claim 13, further comprising a step of
2 performing a vertical implantation into said back gate electrode of an ion
3 species that retards oxidation before said step of oxidation, thereby
4 decreasing the rate of oxidation in the vertical direction.

1 18. A method of forming a double-gate transistor comprising the steps of:
2 providing an SOI wafer having a first substrate, a BOX layer and a device
3 layer;
4 forming a back gate dielectric layer on said device layer;
5 forming a back gate electrode on said back gate dielectric layer;
6 bonding a second wafer having a second substrate to said back gate electrode
7 of said SOI wafer;
8 removing said first substrate;
9 removing said BOX layer;
10 forming a front gate dielectric on said device layer;
11 forming a front gate electrode layer on said front gate dielectric layer;
12 depositing at least one transfer layer on said front gate dielectric;
13 patterning said at least one transfer layer with a gate pattern and forming a
14 first gate in said front gate electrode layer;
15 forming at least one vertical spacer layer adjacent to opposite sides of said
16 first gate;
17 etching said device layer using said at least one spacer layer as a mask to

18 form a transistor body disposed on said back gate dielectric layer;
19 oxidizing said back gate electrode such that oxide is formed below said
20 transistor body and on either side of a central portion of said back gate
21 electrode, thereby forming said back gate self-aligned with said first gate;
22 and
23 forming source and drain electrodes on opposite sides of said transistor body.

1 19. A double-gate transistor formed in a semiconductor wafer having a
2 substrate and a device layer, said transistor comprising:
3 a back gate dielectric layer below said device layer;
4 a back gate electrode below said back gate dielectric layer;
5 a front gate dielectric above said device layer;
6 a front gate electrode layer above said front gate dielectric layer and
7 vertically aligned with said back gate electrode;
8 a transistor body disposed above said back gate dielectric layer, symmetric
9 with said first gate, said back gate electrode having a layer of oxide formed
10 below said transistor body and on either side of a central portion of said back
11 gate electrode, thereby positioning said back gate self-aligned with said front
12 gate; and
13 source and drain electrodes on opposite sides of said transistor body.

1 20. A transistor according to claim 19, in which conductive S/D contact
2 members are disposed above said source and drain electrodes, extending
3 above said front gate dielectric to a contact surface at a height less than said
4 front gate electrode.

